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10/598,519	06/07/2007	Syuji Kimura	SI08-P06593US	6783

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EXAMINER	
BALDRIDGE, BENJAMIN M	

ART UNIT	PAPER NUMBER
2831	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/598,519	KIMURA ET AL.	
	Examiner	Art Unit	
	Benjamin M. Baldridge	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7 June 2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 8 are presented for examination.

Drawings

2. The informal drawings are not of sufficient quality to permit examination. Specifically, lettering indicating the various parts and items in the drawings are not sufficiently legible as to allow clear reproduction, and in some cases are not sufficiently clear to allow examination. For example, signal path between LPF (60) and VCO (20) in Figure 1 is not clearly shown; lettering indicating periods (e.g. Ta, Tb, Tc, etc.) in Figure 2 is illegible; time indications ta, tb, tc, etc. in Figure 7 are not legible. There are numerous other illegible item labels in the various drawings. Accordingly, replacement drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to this Office action. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action.

Applicant is given a TWO MONTH time period to submit new drawings in compliance with 37 CFR 1.81. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a). Failure to timely submit replacement drawing sheets will result in ABANDONMENT of the application.

Specification

3. The disclosure is objected to because of the following informalities:

Page 6, paragraph 2, line 6: the phrase “the locked state is remained” appears to contain a typographical error. For the purposes of examination, the phrase will be read as “the locked state remains”.

Page 7, paragraph 1, line 1, paragraph 2, line 9: the term “whisker-like noises" is unclear. For the purposes of examination, the phrase will be construed to mean “noise spikes”, which is consistent with the general meaning of the term as used in the specification.

Page 10, paragraph 3, line 4: the phrase "of frequency dividing” is unclear. For the purposes of examination the phrase will be read as “of frequency divisions”.

Page 10, paragraph 3, line 8: the phrase “an external separatedly-excited” is unclear. For the purposes of examination, the phrase will be construed as "an external separately-excited".

Page 12, paragraph 1, line 3: reference to “VCO" as “power source voltage VCO” appears to conflict with the use of the term "VCO" to denote a voltage controlled oscillator. From the drawings, it appears that the proper reference should be "VCC", as "power source voltage VCC”, and the term will be so construed for the purposes of examination.

Appropriate correction is required.

Claim Objections

4. Claims 6 and 7 are objected to because of the following informalities:

The limitation “in a predetermined judgment term" is recited in claims 6 and 7, but the meaning of "predetermined judgment term" is unclear. For the purposes of examination,

the phrase will be taken to mean "predetermined period of time". This interpretation is consistent with the specification, and with other uses of the term "term" in the claims, in which the meaning of "term" is clearly "period of time".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 – 3 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirota et al. (US Patent Application Publication Pub. No. US 2004/0027157 A1, Pub. Date February 12, 2004, hereinafter referred to as Hirota).

As to claim 1, Hirota discloses:

A lock detecting circuit that detects whether a PLL circuit is in a locked state based on a phase difference signal supplied from a phase comparator of the PLL circuit ([0074], lines 1 – 6; [0075], lines 1 – 4; Note also Figure 9, items PD 112, LD 122, and 300);

A first circuit that outputs a control signal having one level when the phase difference signal does not indicate a generation of a phase difference, and the other level when the phase difference signal indicates a generation of a phase difference ([0076], lines 1 – 10; note that Hirota explicitly discloses two separate output levels based on whether a phase difference exists);

A second circuit that latches the control signal ([0077], lines 1 – 4; also Figure 9, item 300; note explicit disclosure of latch circuit);

A third circuit that outputs, for a predetermined second term, a lock detecting signal indicating that the PLL circuit is in a locked state, when the latched control

signal indicates the one level for a predetermined first term ([0078], lines 5 – 15; [0076], lines 1 - 5; note explicit disclosure of "predetermined number of times", which is taken to be equivalent to the limitation "predetermined first term" recited in the instant claim).

As to claims 2 and 3, Hirota discloses:

The third circuit measures a term during which the latched control signal continuously indicates the one level and, when the measured term exceeds the predetermined first term in length, outputs the lock detecting signal [claim 2] ([0076], lines 1 – 8. Note explicit disclosure of successive clock inputs, and explicit disclosure of "predetermined number of times", which is taken to be equivalent to the limitation "predetermined first term" recited in the instant claim);

The second term is set to be a term during which the latched control signal indicates the one level [claim 3] ([0078], lines 11 – 15).

As to claim 8, the methods disclosed in the instant claims are intrinsic to the circuit and system disclosed in claims 1 – 3, as discussed above, since the method steps will be met during the normal operation of the system stated above. In addition, note that the steps recited in the instant claim – i.e. creating the control signal based on a phase difference, latching it, and outputting it for a predetermined period of time to indicate that the PLL is in a locked state, are all explicitly disclosed by Hirota, as discussed above with regard to claim 1.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirota in view of Taniguchi et al. (US Patent 5,936,473, August 10, 1999, hereinafter referred to as Taniguchi).

As to claims 4 and 5, Hirota discloses an apparatus as discussed in paragraph 6 above.

Specifically, Hirota fails to disclose:

The third circuit executes the measurement based on a second clock signal phase-inverted from a first clock signal that is used for the latching in the second circuit [claim 4]

The first and the second clock signals are clock signals created from an identical clock source [claim 5].

Taniguchi discloses:

The third circuit executes the measurement based on a second clock signal phase-inverted from a first clock signal that is used for the latching in the second circuit [claim 4] (Figure 2, item CLOCK 45, INTERNAL CLOCK 13; Column 4, lines 65 - 67. Note also that the use of two clocks in phase opposition in a phase lock loop, or lock detecting circuit, or to trigger execution of a circuit function based on phase differences, is well known in the circuit design arts, and would have been obvious to persons of ordinary skill in those arts at the time of the invention; two clocks in phase opposition, summed together, can easily be used to control a phase locked loop or for other purposes, and such a use would have been obvious to persons of skill in the art at the time of the invention);

the first and the second clock signals are clock signals created from an identical clock source [claim 5] (Column 4, lines 65 – 67; the term “identical clock source” is taken to mean “the same clock source", an interpretation well within the broadest reasonable meaning of the term "identical").

Given the teaching of Taniguchi, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the apparatus of Hirota by employing well known or conventional features such a second clock signal phase

inverted from the first, created from an identical clock source, as disclosed by Taniguchi, in order to reliably detect and indicate locking in a phase lock loop circuit.

9. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirota in view of Pierrick (US Patent 6,856,659 B1, February 15, 2005, hereinafter referred to as Pierrick).

As to claims 6 and 7, Hirota discloses an apparatus as discussed in paragraph 6 above.

Specifically, Hirota discloses:

The third circuit outputs the lock detecting signal [claims 6, 7] ([0078], lines 5 - 15);

Hirota fails to disclose:

When the length of the term during which the latched control signal indicates the one level exceeds the length of a term during which the latched control signal indicates the other level, in a predetermined judgment term [claim 6].

When the length of the term during which the latched control signal indicates the one level exceeds the length of the first term that is set to be shorter in length than a predetermined judgment term, in the predetermined judgment [claim 7]

Pierrick discloses:

When the length of the term during which the latched control signal indicates the one level exceeds the length of a term during which the latched control signal indicates the other level, in a predetermined judgment term [claim 6] (Column 2, lines 14 – 24, 33 – 37; Column 6, lines 21 – 36, 53 – 58; Column 7, lines 28 – 35. Note that the apparatus of Pierrick accounts for the duration of pulses as a process of counting the pulses, assigning them to "zones" (taken to be registers for counting the number of occurrences of logical 1 and 0), expressing their values as pulses whose pulse width is proportional to the number of pulses received over a time period, and outputting the result to a comparator (Column 7, lines 28 - 35) and based on the comparison, outputting a control signal).

When the length of the term during which the latched control signal indicates the one level exceeds the length of the first term that is set to be shorter in length than a predetermined judgment term, in the predetermined judgment [claim 7] ((Column 2, lines 14 – 24, 33 – 37; Column 6, lines 21 – 36, 53 – 58; Column 7, lines 28

– 35. Note that reversing the outputs(i.e. inversion of an output) based on relative times of length of a first term versus a judgment term, as taught by Pierrick, is well within the capabilities of persons of ordinary skill in the circuit design arts, and would have been obvious to such persons at the time of the invention).

Given the teaching of Pierrick, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the apparatus of Hirota by employing well known or conventional features such a first term that exceeds the length of a term indicating a state of the lock detector, as disclosed by Taniguchi, in order to prevent false-lock indication and reliably indicate locking in a phase lock loop circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin M. Baldridge whose telephone number is 571 270 1476. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571 272 2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Benjamin M Baldridge/
Examiner, Art Unit 2831

/Timothy J. Dole/
Primary Examiner, Art Unit 2831